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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/565,618	ZINGHER, ARTHUR R.	
	Examiner	Art Unit	
	DAVID J. HUISMAN	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-16 and 19-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-16 and 19-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12, 14-16, and 19-22 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: 371 Documents and Preliminary Amendment as received on 1/24/2006, and Extension of Time and Power of Attorney as received on 5/6/2007.

Information Disclosure Statement

3. The references cited in the PCT Search Report have been considered, but will not be listed on any patent resulting from this application because they were not provided on a separate list in compliance with 37 CFR 1.98(a)(1). In order to have the references printed on such resulting patent, a separate listing, preferably on a PTO/SB/08A and 08B form, must be filed within the set period for reply to this Office action.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

6. The disclosure is objected to because of the following informalities: In paragraph [0002], please insert the serial number of the related application.

Appropriate correction is required.

Drawings

7. The drawings are objected to because Fig.4 includes poor line quality and unreadable text. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

8. Throughout the claims, applicant is inconsistent with the use of dashes. For instance, in claim 1, applicant claims “fast-response” and “fast response”. Similarly in claim 2, applicant claims "low-level” and “low level”. Please ensure that dashes are used consistently.

9. Claim 1 is objected to because of the following informalities: In line 4, the phrase “to extract selectively data” is grammatically incorrect and should be reworded. Appropriate correction is required.

10. Claim 2 is objected to because of the following informalities: In line 4, the phrase “to monitor selectively sustained data” is grammatically incorrect and should be reworded. Appropriate correction is required.

11. Claim 3 is objected to because of the following informalities: In lines 7-8, the phrase “to extract selectively data” is grammatically incorrect and should be reworded. Appropriate correction is required.

12. Claim 12 is objected to because of the following informalities: In lines 7-8, the phrase “to extract selectively data” is grammatically incorrect and should be reworded. Appropriate correction is required.

13. Claim 14 is objected to because of the following informalities:

- In line 10, remove the dash between “central” and “program”.
- In lines 11 and 12, replace “logic” with --circuit--.

Appropriate correction is required.

14. Claim 16 is objected to because of the following informalities: In line 3, replace “steps” with --step--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

15. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

16. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

17. The term "major" in claims 1-3 is a relative term which renders the claim indefinite. The term "major" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Would 1 cycle delay qualify as major time-distortion? 5 cycles? 30 cycles?

18. Claim 7 recites the limitation "the data path" in line 1. There is insufficient antecedent basis for this limitation in the claim because parent claim 2 does not set forth a data path.

19. Claim 12 recites the limitation "the processor's" in line 10. There is insufficient antecedent basis for this limitation in the claim because claim 12 previously sets forth a processor chip, but not a processor.

20. Claims 4-11 are rejected under 35 U.S.C. 112, 2nd paragraph, for being indefinite, because they are dependent, either directly or indirectly, on an indefinite claim.

Claim Rejections - 35 USC § 102

21. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

22. Claim 1-12, 14-16, and 19-22 is rejected under 35 U.S.C. 102(b) as being anticipated by Densham et al., U.S. Patent No. 5,740,449 (herein referred to as Densham).

23. Referring to claim 1, Densham has taught a debugging system, comprising:

a) a processor constructed to execute a software program. See Fig.1, component 1.

b) a fast-response circuit coupled to a low-level asset in the processor. See Fig.10 and note fast-response circuit 26, which is coupled to low-level asset 70.

c) the fast-response circuit configurable to extract selectively data from the low-level asset without major time-distortion of the software program executing on the processor. See Fig.10 and note that circuit 26 reads/extracts data from the asset. Also, there is no indication in Densham that the extraction occurs with major time-distortion of the program execution.

d) a data path constructed to transfer extracted sustained data to an evidence file. See column 14, lines 53-61, and note that the extracted data may be logged (i.e., written to a memory file), so that it may be analyzed at some later time. Clearly, if the data is logged, then it must be transferred along a bus to its destination.

24. Referring to claim 2, Densham has taught a debugging system, comprising:

a) a processor constructed to execute a software program. See Fig.1, component 1.

b) a fast-response circuit coupled to a low-level asset in the processor. See Fig.10 and note that fast-response circuit 25 is coupled to low-level asset 16H, 16V, and the bus coupling the response circuit to the asset.

c) the fast-response circuit configurable to monitor selectively sustained data from the low-level asset for a predetermined event without major time-distortion of the software program executing on the processor. See Fig.10 and note that circuit 25 monitors data on the bus coupling itself to the I/O means. It is checking for a parity error (predetermined event). Also, there is no indication in Densham that the monitoring occurs with major time-distortion of the program execution.

d) wherein the fast-response circuit is constructed to transmit an action signal responsive to the event. See Fig.10 and column 14, lines 11-18. When a parity error event occurs, circuit 25 transmits an action signal (latch signal) to register 70.

25. Referring to claim 3, Densham has taught a debugging system, comprising:

a) a processor constructed to execute a software program. See Fig.1, component 1.

b) a fast-response circuit coupled to a low-level data asset in the processor. See the abstract and Fig.7, and note that circuit 13 is coupled to a low-level asset 35,37 in the processor.

c) the fast-response circuit having a first portion configurable to monitor data from the low level asset for a predetermined event, and constructed to generate an action signal upon the occurrence of the predetermined event. See the abstract and Fig.7 and note that circuit 13 monitors the data from locations A and B for the occurrence of a predetermined event. If the event occurs, then an action signal (interrupt signal) is generated.

d) the fast response circuit having a second portion configurable to extract selectively data from the low level asset and constructed to act responsive to the action signal. See the abstract and note that the data is actually read/extracted from locations A,B. And, in response to the action signal, further action is taken.

e) a data path constructed to transmit extracted sustained data to an evidence file without major time-distortions of the software program executing on the processor. See the abstract and note that in response to the action signal, the extracted data is written to a third memory location (these locations and the corresponding written data forming a file). Also, there is no indication in Densham that the transmission occurs with major time-distortion of the program execution.

26. Referring to claim 4, Densham has taught a system as described in claim 1. Densham has further taught that the low-level asset is constructed as a commit buffer, a reorder buffer, a high-speed data bus, or a register. Note that the low-level asset 70 in Fig.10 is a register.

27. Referring to claim 5, Densham has taught a system as described in claim 1. Densham has further taught that the fast response circuit is integrated on-chip with the low-level asset of the processor. See Fig.1, Fig.2, and column 1, line 41, to column 2, line 12. Note that the processor 1, as a whole, comprises multiple arrays of processing unit (cards), and each card comprises the control processor/fast-response circuit shown in Fig.10. Therefore, the components are integrated on the processor chip.

28. Referring to claim 6, Densham has taught a system as described in claim 1. Densham has further taught that the fast response circuit comprises high-speed registers. Furthermore, the fast response circuit 26 of Fig.10 inherently includes registers because registers are an inherent component of a processor.

29. Referring to claim 7, Densham has taught a system as described in claim 1. Densham has further taught that the data path comprises one or more resources of the processor's hierarchy. As previously discussed, the extracted data is written to a memory for later analysis. Hence, the data path comprises a resource from the processor's memory hierarchy.

30. Referring to claim 8, Densham has taught a system as described in claim 3. Densham has further taught:

a) sequential logic connected to the first portion of the fast response circuit. It is inherent that the monitoring portion (first portion) of the response circuit includes sequential logic.

b) wherein the sequential logic is programmable to selectively monitor for program events, and the sequential logic enables an action responsive to the compound program events. See the abstract and note that there are multiple events which may signal interrupts. Since there a multiple events, these could be collectively referred to as compound process events.

31. Referring to claim 9, Densham has taught a system as described in claim 3. Densham has further taught:

a) sequential logic connected to the second portion of the fast response circuit. It is inherent that the signaling portion (second portion) of the response circuit includes sequential logic.

b) wherein the sequential logic is programmable to selectively extract data. See the abstract and note that the sequential logic will or will not extract data for writing to memory based on whether the data from locations A and B cause an interrupt to occur.

32. Referring to claim 10, Densham has taught a system as described in claim 8 or 9. Densham has further taught that the sequential logic is constructed as a co-processor. Clearly, the sequential logic performs some processing. And, according to claim 8, Fig.7 is separate from

processor 26 of Fig.10. So, in essence, the sequential logic is a coprocessor with respect to processor 26 in Fig.10.

33. Referring to claim 11, Densham has taught a system as described in claim 8 or 9. Furthermore, looking at Fig.1, component 1, every component is integrated into the processor chip.

34. Referring to claim 12, Densham has taught a debugging system, comprising:

a) a low-level asset. See Fig.7, components 35, 37 (ALU inputs/operands).

b) a fast-response circuit coupled to a low-level data asset in the processor. See the abstract and Fig.7, and note that circuit 13 is coupled to a low-level asset 35, 37 in the processor.

c) the fast-response circuit having a first portion configurable to monitor data from the low level asset for a predetermined event, and constructed to generate an action signal upon the occurrence of the predetermined event. See the abstract and Fig.7 and note that circuit 13 monitors the data from locations A and B for the occurrence of a predetermined event. If the event occurs, then an action signal (interrupt signal) is generated.

d) the fast response circuit having a second portion configurable to extract selectively data from the low level asset and constructed to act responsive to the action signal. See the abstract and note that the data is actually read/extracted from locations A,B. And, in response to the action signal, further action is taken.

e) a data path including one or more resources of the processor's hierarchy, the data path constructed to transmit sustained evidence data to an evidence file. See the abstract and note that in response to the action signal, the extracted data is written to a third memory location (these locations and the corresponding written data forming a file).

35. Referring to claim 14, Densham has taught a processor comprising:

a) a low level asset. See Fig.10, component 70.

b) a fast response circuit. See Fig.10, components 25 and 26.

c) a high speed data path constructed to transfer sustained data from the low level asset to the fast response circuit. See Fig.10, and note the data path between the low level asset 10 and the fast response circuit portion 26.

d) wherein the processor performs the steps of:

d1) executing a central program. Processors inherently execute programs.

d2) detecting the event using the fast response logic. See column 14, lines 29-33, and note that the fast response logic detects an interrupt event is occurring by receiving an interrupt signal on bus 65 (Fig.10).

d3) extracting data selectively using the fast response logic. See column 14, lines 29-33, and Fig.10, and note that the circuit reads/extracts data from the asset.

d4) transferring the extracted data to a memory. See column 14, lines 57-61, and note that the data may be logged/stored in memory.

d5) wherein the detecting, extracting, and transferring steps are performed without major time-distortion of the central program executing on the processor. There is no indication in Densham that the aforementioned steps occur with major time-distortion of the program execution.

36. Referring to claim 15, Densham has taught a processor as described in claim 14. Densham has further taught:

a) a second low level asset connected to the fast response circuit. See Fig.10, components 16H, 16V, and the bus coupling 16H and 16V to the parity checker 25 (a portion of the fast response circuit).

b) wherein the extracting step includes selectively extracting data from the second low level asset. It is the job of the parity checker to extract data from the bus and ultimately from components 16H and 16V to determine parity errors in data.

37. Referring to claim 16, Densham has taught a processor as described in claim 14. Densham has further taught:

a) a sequential logic circuit connected to the fast response circuit. See Fig.10, components 68 and 70.

b) wherein the processor performs the steps of transmitting an action signal to the sequential logic responsive to detecting the event. When a parity error is detected by parity checker 25, a signal is sent to the sequential circuit so that the current count is latched.

38. Referring to claim 19, Densham has taught a debugging system, comprising:

a) a processor constructed to execute a software program and having a shared high- speed data transfer bus. See Fig.1, component 1. Also, note that a processor is inherently coupled to a high-speed bus for communication purposes.

b) a fast-response circuit coupled to a low-level asset in the processor. See Fig.10 and note fast-response circuit 26, which is coupled to low-level asset 70.

c) the fast response circuit configurable to extract sustained data from the low-level asset. See Fig.10 and note that circuit 26 reads/extracts data from the asset.

d) a high-speed data path extending to an evidence file, the high-speed data path including the

shared high-speed data transfer bus. See column 14, lines 53-61, and note that the extracted data may be logged (i.e., written to a memory file), so that it may be analyzed at some later time. Clearly, if the data is logged, then it must be transferred along a bus to its destination.

39. Referring to claim 20, Densham has taught the debugging system according to claim 19, wherein the high speed data path further includes one or more resources of the processor's hierarchy. As previously discussed, the extracted data is written to a memory for later analysis. Hence, the data path comprises a resource from the processor's memory hierarchy.

40. Referring to claim 21, Densham has taught the debugging system according to claim 19, wherein the fast response circuit is constructed to extract the sustained data without major time-distortion to the software program executing on the processor. There is no indication in Densham that the extraction occurs with major time-distortion of the program execution.

41. Referring to claim 22, Densham has taught the debugging system according to claim 19, wherein the high-speed data path is constructed to transfer the sustained data to the evidence file without major time- distortion to the software program executing on the processor. There is no indication in Densham that the transfer occurs with major time-distortion of the program execution.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID J. HUISMAN whose telephone number is (571)272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David J. Huisman/
Primary Examiner, Art Unit 2183
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